A Review on Nano Transistor Applications of Layered Dithioxotungsten

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Abstract

Dithioxotungsten is chemically known as Tungsten disulfide (WS_2) and is known for its superlubrication. In this review article, the performance of dithioxotungsten (WS_2) as a channel material in nanotransistors is analysed based on the performance of WS_2 on regard of mobility of charge carriers, on/off ratio of transistors, channel width to length ratio, channel thickness and, I-V characteristics and transistor performance.

Key words: Dithioxotungsten, WS_2, Nano Transistors

1. Introduction

Graphene as a two-dimensional material is having high mobility, but its non-bandgap nature limits the implementation of 2D geometry in certain areas such as transistors and sensors [1]. Transition Metal Dichalcogenides (TMDs) are one of the most adaptable materials due to their wide variety of physicochemical, electrical and mechanical properties that lie in between the semiconductor and metal[2]. Beyond TFTs, FETs are proposed as the high-performance devices. For the

fabrication of the field effect transistors (FETs) graphene can be used but, it is not a promising candidate as it lacks bandgap and can't be used as active channel. Although bandgap can be introduced and tuned by fabricating graphene in to nano ribbon form[3], functionalization with different chemical elements[4], using bilayer graphene[5] etc. But the complexity of fabrication and degradation of mobility is arising with serious questions about the device performance like drastic lowering of on/off ratio[6]. Two dimensional dichalcogenides is the best alternative candidates and these are better alternatives compared to graphene-based FETs because of its bandgap ranges from 1- 2 eV[7]. Among them Tungsten based dichalcogenide 2D materials show promising thickness dependent electronics band structure. These materials exhibit comparatively high carrier mobility[8-9]. Among the Tungsten based 2D dichalcogenides WS_2 shows the characteristic behaviour such as transition from indirect bandgap to direct band gap material when it is peeled down to mono layers[10-11]. WS_2 as bulk material shows an indirect bandgap of 1.4 eV and it's monolayer shows a direct bandgap of 2.1 eV[12-13].

WS_2 is a layered transition metal dichalcogenide (TMDC)[14-17]. WS_2 exhibit high photoluminescence when exfoliated in bi/few layers[14-17]. The optical bandgap of WS_2 shows a change from indirect, 1.3 – 1.4 eV to direct, 1.8 – 2.1 eV in mono/bi layers[12-17]. In direct bandgap structures the mobility and conductivity of charge carriers in WS_2 can be tuned by application of external field[12-17]. This property makes WS_2 a potential candidate to be applied in field effect thin film transistors. As the thickness of single layer WS_2 is of the order of 0.7 nm, exploring single/bi/few layers of WS_2 as channels in transistors for charge transport, great miniaturization of the device can be actualised[17-19]. Exploration of flexible nanotransistors is a trending field in semiconducting material research. The electrical properties of TMDCs vary from insulating to metallic behaviour based on transition metal d-electrons and crystal structures[20-22]. As tungsten is one of the most abundant elements in the earth's crust and also very dense and cost effective it is interesting to study the properties of WS_2.

Among all TMDCs WS_2 shows more semiconducting behaviour for thin film transistor applications because of huge photoluminescence, direct bandgap, mechanical flexibility, chemical stability, large in-plane carrier mobility, high spin orbit coupling energy of about 420 MeV, large exciton binding energy and a high mobility of the order of 300 $cm^2/V\text{-}s$[23-26]. Monolayer WS_2 is well studied for transistor applications due to excellent carrier mobility, as well as its potential applications in spintronics, valleytronics, energy-storage, sensing, electronic and photonic devices applications[12-26]. WS_2 is having many properties, like the transition

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of indirect to direct bandgap, layer-dependent bandgap, large exciton binding energy, strong spin–orbit splitting, valley selection etc. and shows good stability at ambient conditions. It is exhibiting higher quantum efficiency, wider valence band maximum splitting and, lower effective mass of the carrier due to the presence of heavier tungsten atom[12-26].

Influence of methods of preparation like mechanical exfoliation, liquid exfoliation, pulsed laser deposition, chemical vapour deposition, physical vapour deposition, e-beam evaporation etc., are found to alter the optoelectronic properties of WS_2 [27-35]. The design of transistor, like the position of the gate terminal, which is classified into top contact and bottom contact structures are also affecting the performance of the transistors[36-37]. Due to the large injection area in top contact structures, the field effect mobility is found to be higher and contact resistance is lower[36-37]. But due to poor morphology in bottom contact structures the mobility is lower[36-37]. Top contact structures show good performance due to the reduced contact resistance at the source and drain electrodes[36-37]. The performance of TFT is also depending on the techniques of doping of the channel material, the choice of the substrates, the selection of contact materials and contact resistance[36-37]. An on/off ratio of 10^5 to 10^7 is reported in the case of WS_2 in various deposition conditions of the channel material and design of TFT, with a mobility of 13 to 489 cm/V-s[6, 38-39].

In this review article, the performance of dithioxotungsten (WS_2) as a channel material in nano transistors is analysed based on the performance of WS_2 on regard of mobility of charge carriers, on/off ratio of transistors, channel width to length ratio, channel thickness and, I-V characteristics and transistor performance.

WS_2 – Analysis as a versatile optoelectronic material

Dithioxotungsten consists of S-W-S sandwich pattern, as shown in figure 1, of atoms arranged in a trigonal prismatic configuration [40]. The crystal lattice of 2-H WS_2 belongs to the non-symmorphic hexagonal space group $P6_3/mmc$ (D_6h_4) which has the space inversion symmetry[41-42]. Single layer has 1H structure[41]. Monolayer WS_2 belongs to P_6m_2(D_3h') group[41]. Even layer WS_2 has the space inversion symmetry while odd layer WS_2 lacks the space inversion symmetry[41]. The conduction band minimum (CBM) and the valance band maximum (VBM) are both located at K point in monolayer WS_2. When the layer number of WS_2 increases, the VBM shifts to Γ point, while the CBM locates between K and Γ points (called Q point) [41]. The band edge states at K point have dominant contributions from the tungsten d(x_2-y_2), d_{xy}, and d_z^2 orbitals with an admixture of the S p-orbitals[41]. For the states at Q_c and Γ_v, the contribution from the S p_z orbitals become significant,

which plays an important role for the transition from direct to indirect bandgap from monolayer to bilayer and multilayer[41].

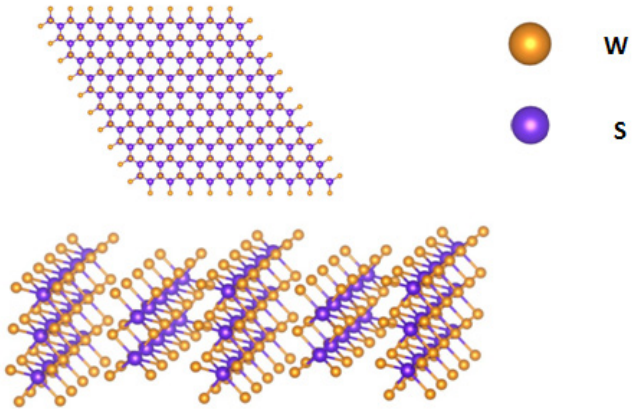

Figure 1: S-W-S pattern of WS_2

The transition from a direct bandgap (monolayer WS2) to an indirect bandgap (bilayer and multilayer WS_2) is a consequence of the spin-orbit coupling (SOC) and interlayer hopping[41-43]. Greater SOC in WS_2 results in spin–orbit splitting of the valance band of the order of 400 meV near the valence K point[41-43]. Tungsten d_{xy} and $d_{(x^2 - y^2)}$orbitals are highly localized in individual layers, due to this, VB splitting near the K point is dominated. The spin–orbit splitting energy has not much changes with the number of layers in the sample, as interlayer hopping of orbitals is comparatively lower[41]. In the case of monolayer WS_2 samples, splitting of the VBM can be associated with the lack of inversion symmetry and also the spin–orbit effect. But the corresponding splitting in the case of bilayer is due to the combination of interlayer interaction and SOC.

Due to the large SOC, the VBM of monolayer WS_2 exhibit the spin-index locked with the valley- index. The VBM valley K or -K has only the spin up or down electrons respectively. This leads to the valley-dependent optical selection rules. As per the selection rule, the circularly polarized light can selectively excite the K or -K valley electrons from the spin-polarized bands. The interlayer hopping energy in WS_2 is of the order of 0.1 eV, which is lesser than the spin–valley coupling strength in WS_2which is of the order of 0.4 eV[41].

Exciton in WS_2 is highly confined to the plane of the ML. With change in

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dielectric atmosphere, both the electron and hole experience a reduced screening effect. Hence the bandgap is expected to increase for monolayer WS_2 (2.7 eV). With the exciton binding energy (0.7 eV), an enhanced electron–hole interaction can be expected[42].

Raman scattering is a very good tool for confirmation of formation of WS_2. The major vibrational modes of WS_2 can be analysed with Raman scattering experiment. Longitudinal Acoustic (M) at 176 cm^{-1}, Doubly degenerated E_{2g} mode at 356 cm^{-1}, 2LA(M) mode at 352 cm^{-1} and singly degenerate A^1_g at 418 cm^{-1} are major vibrational modes of WS_2. There will be shift in the peak position, appearance of shoulder peaks and change in the intensityof peaks depending on the number of layers in the sample, defects in the material, adsorption etc. Peak separation gives information about number of layers, deformation/splitting in peak gives information about strain/defects/adsorption in material[44-46].

Synthesis methods of WS_2 mono/few layers include methods like mechanical exfoliation – peeling/ scotch tape method, chemical vapor deposition, sputtering, atomic layer deposition, liquid phase exfoliation – laser ablation, ultrasonic method, molecular beam epitaxy, spin coating – on different substrates like titanium-titanium dioxide, graphite, silicon-silicon dioxide, graphene oxides, gold foil, h-boron nitride, sapphire etc. Chemical vapour deposition, especially the epitaxial one, has added advantages. In the samples grown through epitaxial method, the defect density is lower. Its possible to develop large area samples through this method. The electrical conductivity of CVD grown samples exhibit more endurance in-plane level[27-35].

To achieve definite applicability, growth techniques need to control more finely, the size, layer thickness/ numbers, edge sharpness, the phase purity of the grown crystals and defects that may arise in the sample during growth process. Growth techniques influences the edge structure of the grown WS_2, ie., whether the sample edge is metal or chalcogen. This influences the carrier density distribution in and near the fermi energy level. It also affects how much the atomic orbitals overlap[41]. Profile of band-edge can be modified while growth using various band-structure engineering mechanisms. Bandgap can be modified by keen control of composition of alloy during synthesis[41]. In the case of heterostructures with no common species or dissimilar band profiles or with different lattice patterns, quantum engineering can be adopted for bandgap modification[41]. Combinations of different morphologies of lateral-vertical heterostructures can be developed, to contribute to the active channel layer of nanotransistors[41].

3. WS_2 – Application as a channel material in Transistors

Field effect transistors based on WS_2 as channel layer show a large on/off ratio of greater than 10^5. Large bandgap of two dimensional WS_2 can cause large on/off ratio[47]. Theoretically, the mobility of carrier in WS_2 channel could be high, the practically measured mobility is relatively low. Many factors like, the dielectric environment, percentage and type of defects and influence of adsorbents, can influence the performance of WS_2 as a channel material in transistors. The transport properties are highly influenced by number of layers and kind of stacking[48]. Process of adsorption when exposed to atmosphere is also influencing the performance of WS_2 channels. Hydrogen, water molecules and oxygen when get adsorbed to the surface of WS_2 cause p- type doping[49-51]. It has both advantage or disadvantage, as WS_2 can be used as an ambipolar material, at the same time, when mono/few layer TFT is exposed in air may exhibit weak p-type or n-type behavior[49-51]. Conductivity type can be modified from n-type to p-type in high pressure atmosphere of adsorbates[49-51].

A schematic diagram of basic TFT architecture is shown in figure2, in which substrate can be solid substrates like silicon and flexible substrates like polyamide. Saptarshi Das et.al[52] successfully fabricated monolayered WS_2 on silicon (P++ Si) substrate with back gate architecture. Thermally grown SiO_2 of 100 nm over Si is served as the dielectric/ insulating layer. A CVD grown WS_2 on titanium (Ti) substrate which was transferred through PMMA transfer technique in which initially PMMA will be coated over WS_2- Ti substrate, then the entire substrate will be submerged in 1M NaOH until monolayer and PMMA fill get detached and remain in the solution, fully separated from Ti substrate. Then the entire PMMA with 2D WS_2 material was transferred on the Si/SiO_2 substrate. Then 40-50 nm Ni/Au source drain contacts made through e-beam lithography. Other architecture on flexible substrate include Polyamide, has been demonstrated by Thomas. N. Jackson et.al [53]. In their work a 100 nm Ti gate electrode array was deposited by sputtering and it was patterned photolithographically on polyamide substrate, and followed by a lift off process. A Plasma Enhanced Atomic layer deposition (PEALD) of Al_2O_3 is then carried out at 200 °C as the gate dielectric / insulator layer for the device. A few layers of WS_2 2D material is then transferred from Si substrate to patterned polyamide substrate by using PMMA transferring technique. A 50 nm Au source-drain contacts made by thermal evaporation and followed by photolithography procedure. A 30 nm $Al_2O_3$is then deposited over the device by ALD technique to encapsulate the device. Britnell et. al[54] also fabricated field effect tunnelling transistor with a more complex 2D

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heterostructure, with entire stack with layered materials on flexible transparent substrates.

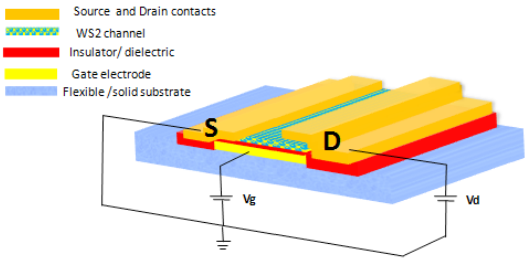

Figure 2: Schematic diagram of basic TFT architechture with WS_2 channel

Effect of number of layers of WS_2 on the performance of TFT is tabulated in table 1. In bilayer morphology, carrier mobility in WS_2 TFT is 300 cm^2 /V-s according to Palummo et. Al[55], which is greater than that of 140 cm^2 /V-s monolayer channel (Nayak et. al)[56]

Table1. Effect of number of layers of WS_2 in channel of TFT

Layers	Type	Band gap energy eV	Photolumi-nescence	Mobility (cm^2/Vs)	Carrier con-centration	Ref.
Bulk WS_2	Indirect	1.3 - 1.4	Absent	255	n - type	Lan et al.[41]
Bilayer WS_2	Direct	1.800	Strong	300	p - type or n - type	Lu qet al.[55]
Monolayer WS_2	Direct	2.1	Less	140	n - type	Nayak. et al. [56]

Growth techniques influence the performance of TFT in many aspects. So, bandgap engineering, quantum engineering, phase pure growth, large area growth, single layer growth etc. plays greater role in the performance of TFT. Metal edge or chalcogen edge, sulphur vacancy etc. alters the mobility of carrier. Hwang et. al has reported an on/off ratio of 10^5 on scotch -tape peeled WS_2 layer[57]. Jiang et. al[58] reports nitrogen plasma treatment to reduce sulphur vacancy caused deficiency. Treating with nitrogen plasma enhanced the mobility from 29.7 to 184.2 cm^2/V-s

and on-off ratio from 10^3 to 10^6. TFT on nitrogen plasma treatment result in ohm-like contact and exhibit linear I_{DS}–V_{DS} pattern near 0 V. S vacancies may result in reduced charge scattering. Nitrogendoping may result in reduced effective carrier mass and enhanced mobility[57-58]. Effect of growth techniques is tabulated in table 2[57-63]. A large on-off ratio of 10^7 is reported on a h-BN substrate grown through CVD method by Illarionov et al. A large mobility of 486 cm^2/V-s in the same structure at 5 K is also reported[57-63].

Table 2. Effect of growth techniques of WS_2 on mobility and on-off ratio

Method	Sub-strate	Characteristics	Ohmic Contact	Mobility [cm^2/Vs]	On/Off Current Ratio	Ref.
Scotch tape method	SiO_2	Clean	Ti / Al	30	10^5	Hwang*et al.*[57]
Fast pulsed I-V method	Si / SiO_2	Temperature instability	Ni / Al	44	10^6	Iqbal*et al.*[58]
Liquid phase exfoliation		Simplest cost effective, high deposition rate, purity, low capital cost material.			10^6	Ott *et al.* [59]
CVD	SiO_2	High performance. Large area production	SiO_2	80	10^6	Wu*et al.* [60]
CVD	h-BN	High uniformity. Hysteresis absent	Al / Au	185 at room temp. 486 at 5 K	10^7	Illarionov *et al.*
Mechanical exfoliation	h-BN	Low yield, low scattering impurities. Small size, high quality	Al	0.30	4.56 × 10^6	Kumar*et al.*
E beam evaporation	SiO_2	Better stability and electrical performance	Ni	27.90	10^6	Wu *et al.*
HPHA	Si / SiO_2	Low contact resistance	Ti / Au	13.00	10^5	Yang *et al.*

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Chemical functionalization with thiol also increases the carrier mobility, the low temperature mobility is reported to increase from 140 to 337 $cm^2/ V-s$[64] and the ambient temperature mobility from 49 to 83 $cm^2/V-s$[64]. The device mobility can also be limited due to defect states in SiO_2 layer in the substrate as it leads to the localization of charge carriers[64]. Hexagonal boron nitride could be a better alternative to avoid such defects and localization of charges. It is having atomically planar surface, high bandgap and low charge impurity density according to Iqbal et. Al[65].

Contact materials also influences the performance of TFTs. The nature of contact materials determines the amount of charge injection and collection between the WS_2 channel and the electrodes. An ohmic contact is more ideal for transistors, but it is very difficult to realize this in single/ bilayer channel materials[66]. The Fermi level pinning caused by interfacial states, results in mismatch of work function between the channel material and the electrode material. To reduce the contact problems, various techniques like annealing, doping, using metal interface layers, using graphene-based electrodes, using edge contacts etc. are being reported by various groups[67].

Length to width ratio of the channel is a very important parameter which influences the performance of TFT. For a channel width of less than 100 nm, the threshold voltage was reported to increase suddenly with abrupt decrease in on-current. Channel size highly determines the hysteresis behaviour. Performance of TFT is dependent on the channel thickness and in the case of WS_2, peak performance is reported in thickness range 6 -10 nm[68].

The design of TFT itself is a deciding parameter in the performance of TFT whether it is top gated or bottom gated. Figure.3 demonstrates the schematic diagram of general design of top gated WS_2 FET architecture. In thisa high quality of thermally grown polished surface of SiO_2 on Si substrate is represented for basic top gate architecture using WS_2 monolayer as channel in FET. Electron beam lithography patterned source and drain contacts can be made through deposition of Cr/Au or Ti/Au in which Cr can be of 5 nm for the better adhesion and, Au or Ti can be of 50 nm thickness. Contact deposition can be preferably done by thermalevaporation method or else by sputter deposition method. For WS_2 FETs, Cr/Au and Ti/Au contacts basically show ambipolarity in nature through which both P-type and n-type injection is possible. For P-type source and drain contacts high work function materials such as platinum can be depositedof thickness about

40-50 nm and a 50-60 nm thick Au can be deposited over Pt as the contact pad extension purposes.

Also, it has been reported that Ni/Au contacts of 40, 50 nm respectively deposited in the case of WS_2 FETs on sapphire substrate in back gate architecture[69]. There are reports which mention annealing of contacts under Argon/ H_2 flow for the improvement of better contact resistance[69-70]. Gate electrodes can be fabricated with electron beam lithographically patterned and then Al_2O_3 of 15 -30 nm can be deposited with Atomic Layer deposition Technique (ALD), and then Au of 50-60 nm again deposited over the dielectric material. Tae Wan Kim et.al[71] fabricated a similar architecture but with ion top gate over WS_2 film FET. There are other different gate dielectric materials already reported with the 30 nm of HfO_2, 30nm SiO_2, 20 nm of h-BN (hexagonal boron Nitride) and then Au of 50-60 nm over the dielectric layer[38].

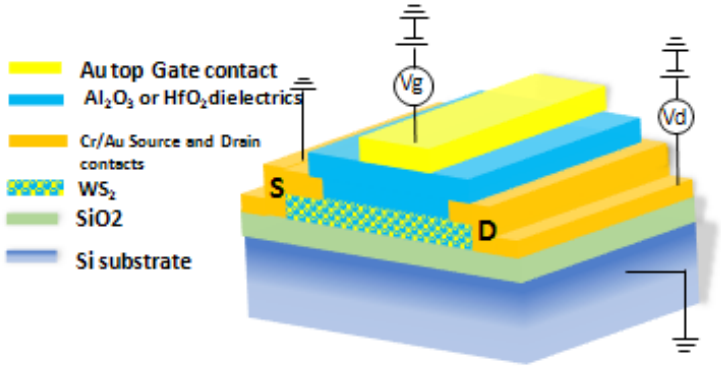

Figure 3: Top gate WS_2 architecture

Figure 4 demonstrates the general bottom gate FET architecture. Bottom gate architecture of WS_2 FETs can be fabricated with both highly doped n or p silicon substrates (n++/ P++ Si). A high quality thermally grown SiO_2 can be deposited over the Si substrates and then the source and drain contacts can be made with above mentioned n-type or p-type contacts or ambipolar contacts. Bottom side of the substrate will act as common gate for the device. A dielectric gate material of

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hexagonal boron nitride h-BN over Si/SiO_2 and WS_2 is transferred over these thin layered h-BN and source-drain contact can made through e-beam lithography with Al/Au contacts. h-BN is used as the gate material in back gate WS_2 FET architecture is also reported[65, 72]. A complex vertical heterostructure like, WS_2-SnS_2 is reported in tunnelling field effect transistors with back gate architecture[73]. Table 3 shows the advantages of different designs of WS_2 based TFT structures[63,74-76].

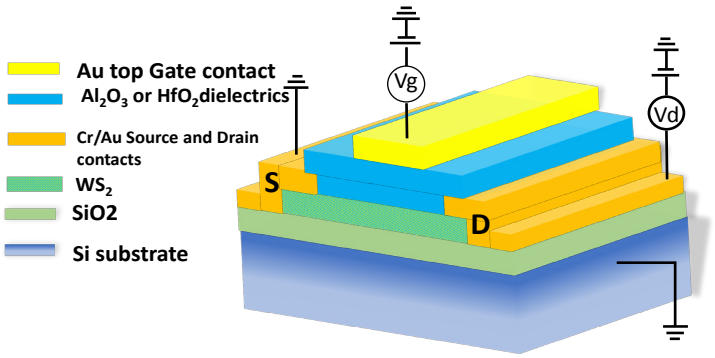

Figure 4: Bottom gate WS_2 transistor architecture

Table 3. Advantages of Bottom/ Top contact designs of TFT

Bottom Contact Structure	Top Contact Structure	Reference
Channel resistance decreases with channel length	Channel resistance increases with channel length	Mittal *et al.*[74]
Mobility is less	Elevated saturation mobility	Abuzaid*et al.*[75]
High morphological disorder	Low morphological disorder	Mittal *et al.*[74]
Low drain current	High drain current	Yang *et al.* [63]
Low transconductance	High transconductance	Yeh *et al.*[76]

Conclusion

Dithioxotungsten chemically known as Tungsten disulphide (WS_2) is very good channel material to be applied in field effect transistors with high carrier mobility of upto 486 cm^2 / V-s at 5 K in bilayer thickness. In mono/bilayers it is a direct bandgap material with ample photoluminescence to be applied in optoelectronic devices. In this review article the performance of dithioxotungsten (WS_2) as a channel material in nano transistors is analysed based on the performance of WS_2 on regard of mobility of charge carriers, on/off ratio of transistors, channel width to length ratio, channel thickness and I-V characteristics. The material property of WS_2like the space group to which WS_2 belongs to, spin-orbit coupling in WS_2, Excitonic nature in WS_2, Raman vibrational modes, etc. which demonstrates WS_2 as most adaptable transition dichalcogenide is also discussed. General top-gated and bottom-gated design for fabrication of WS_2 channel transistor is also demonstrated.

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